Amendments to the Specification

JB

Please replace Page 7, lines 14 to ~~20~~ 21 as follows:

Figure 2 is a block diagram of the encryption processor unit according to one embodiment of the present invention. The EPU 16 includes a decode unit 30, an execution unit 32, and a memory 35. The memory 34 contains a register set 35 which includes registers R1 through Rn. The execution unit 32 includes a plurality of multiplier units 36a through ~~36n, an~~ 36n and an adder 38. During operation, the ~~decoder~~ decode unit 30 receives a request for establishing an SSL session from a client. When this occurs, the decode unit 30 fetches the values N, ~~d and C~~ d, and C from system memory 14 and issues the appropriate micro-instructions so that the M can be computed in the execution unit 32.

Please replace Page 9, lines 4 to 20 as follows:

Figure 3 is a diagram illustrating the cycles used to execute a product operation in an implementation of the encryption processor of the present invention having two multipliers and one adder. Consider the product of the operands (a1, a0) and (b1, b0). In the first cycle, the decode unit 30 issues an instruction (Mult R1 a1,b1 a0,b0). With this instruction, the (a1, b1) and (a0, b0) are simultaneously multiplied using multipliers 36a and 36b respectively. The results of the instruction are then stored in a Register R1. In the second cycle, the decode unit 30 issues another multiplication-add-carry instruction MAC R2 (a1 b0), R1. With this instruction, a1 and b0 are multiplied and the product is added to the contents of R1 and stored in R2. In the third cycle, the decode unit 30